

AMENDMENTS TO THE CLAIMS:

Complete Listing of Claims

1 1. (original) A mixed-signal core designed for efficient testing, comprising:
2 an analog module having a plurality of analog components and a plurality
3 of mixed-signal components;
4 a first digital module having a first plurality of digital components required
5 for functional/parametric verification of the plurality of mixed-signal components
6 within the analog module;
7 a first virtual boundary coupled between the analog module and the first
8 digital module, the first virtual boundary having at least one multiplexer to gate a
9 plurality of signals transmitted between the analog module and the digital
10 module, wherein the first virtual boundary partitions the analog module from the
11 digital module, each of the at least one multiplexer coupled to receive the
12 plurality of signals generated by the plurality of analog and the plurality of mixed-
13 signal components of the analog module and the first plurality of digital
14 components of the digital module;
15 a second digital module having a second plurality of digital components;
16 and
17 a second virtual boundary having at least one multiplexer to gate a
18 plurality of signals transmitted between the first and the second digital module,
19 wherein the second virtual boundary partitions the first digital module from the
20 second digital module, each of the at least one multiplexer coupled to receive the
21 plurality of signals generated by the first plurality of digital components and the
22 second plurality of digital components;
23 wherein the structure for testing has at least three modes of operation for
24 testing the mixed signal core, a first mode of operation that provides digital

25 interface characterization testing of the first and second digital module and
26 analog characterization/trimming testing of the analog module, wherein, in the
27 first mode of operation, the first virtual boundary and the second virtual boundary
28 are inactive;

29 wherein a second mode of operation that provides concurrent testing of
30 the analog module, the first digital module, and the second digital module,
31 wherein analog characterization/trimming testing is performed on the analog
32 module and digital interface characterization testing is performed on the first
33 digital module, while SCAN/BIST testing is performed on the second digital
34 module, wherein, in the second mode of operation, the second virtual boundary
35 is activated to gate the plurality of signals transmitted between the first digital
36 module and the second digital module;

37 wherein a third mode of operation that provides non-concurrent
38 testing of the analog module, the first digital module, and the second digital
39 module, the third mode of operation supplies SCAN/BIST testing of the first and
40 second plurality of digital components from the first digital module and the
41 second digital module, while the analog module is powered down, and wherein,
42 in the third mode of operation, the first and second virtual boundaries are
43 activated to gate the plurality of signals transmitted between the first digital
44 module and the analog module and to gate the plurality of signals transmitted
45 between the first digital module and the second digital module, respectively.

2. (currently amended) A structure for testing an integrated circuit chip having an analog core, a mixed-signal core, a digital core, a microprocessor core, and a memory core therein, comprising:

wherein the mixed-signal core comprises:

an analog module having a plurality of analog components and a plurality of mixed-signal components,

a first digital module having a first plurality of digital components required for functional/parametric verification of the plurality of mixed-signal components within the partitioned analog module,

a first virtual boundary coupled between the analog module and the first digital module, the first virtual boundary having at least one multiplexer to gate a plurality of signals transmitted between the analog module and the digital module, wherein the first virtual boundary partitions the analog module from the digital module, each of the at least one multiplexer coupled to receive the plurality of signals generated by the plurality of analog and the plurality of mixed-signal components of the analog module and the first plurality of digital components of the digital module,

a second digital module having a second plurality of digital components, and

a second virtual boundary having at least one multiplexer to gate a plurality of signals transmitted between the first and the second digital module, wherein the second virtual boundary partitions the first digital module from the second digital module, each of the at least one multiplexer coupled to receive the plurality of signals generated by the first plurality of digital components and the second plurality of digital components;

wherein the structure for testing has at least three modes of operation for testing the mixed-signal core, a first mode of operation that provides digital

30 interface characterization testing of the first and second digital module and
31 analog characterization/trimming testing of the analog module, wherein, in the
32 first mode of operation, the first virtual boundary and the second virtual boundary
33 are inactive;

34 wherein a second mode of operation that provides concurrent testing of
35 the analog module, the first digital module, and the second digital module,
36 wherein analog characterization/trimming testing is performed on the analog
37 module and digital interface characterization testing is performed on the first
38 digital module, while SCAN/BIST testing is performed on the second digital
39 module, wherein, in the second mode of operation, the second virtual boundary
40 is activated to gate the plurality of signals transmitted between the first digital
41 module and the second digital module;

42 wherein a third mode of operation that provides non-concurrent testing of
43 the analog module, the first digital module, and the second digital module, the
44 third mode of operation supplies SCAN/BIST testing of the first and second
45 plurality of digital components from the first digital module and the second digital
46 module, while the analog module is powered down, and wherein, in the third
47 mode of operation, the first and second virtual boundaries are activated to gate
48 the plurality of signals transmitted between the first digital module and the analog
49 module and to gate the plurality of signals transmitted between the first digital
50 module and the second digital module, respectively;

51 wherein the microprocessor core for executing microprocessor
52 instructions multiple times and evaluating the results to ensure integrity of the
53 microprocessor core and for testing the memory core by generating a memory
54 test pattern by the memory core and evaluating the results; and

55 a host computer for providing an executable test program to the
56 microprocessor core through an interface circuit;

57 wherein the analog module and the first digital module are provided with a
58 test pattern for characterization testing generated by the microprocessor core

59 and the resultant output of the analog module and the first digital module are
60 evaluated by either the microprocessor core or the host computer;

61 wherein the first and second digital module are provided with a test
62 pattern for SCAN/BIST testing generated by the microprocessor core and the
63 resultant output of the first and second digital module are evaluated by either the
64 microprocessor core or the host computer.

1 3. (original) A structure for testing a integrated circuit chip as recited in claim 2,
2 wherein the test program applied to the microprocessor core is an object code of
3 assembly language test program.

1 4. (original) A structure for testing a integrated circuit chip as recited in claim 3,
2 wherein the assembly language test program is provided to the microprocessor
3 core from an external host computer through an I/O interface.

1 5. (original) A structure for testing a integrated circuit chip as recited in claim 3,
2 wherein the assembly language test program is provided to the microprocessor
3 core from an external IC tester through an I/O interface.

1 6. (original) A structure for testing a integrated circuit chip as recited in claim 2,
2 wherein the integrated circuit chip is a system-on-chip (SoC) IC.

1 7. (original) A mixed-signal core designed for efficient testing, comprising:
2 an analog module having a plurality of analog components and a plurality
3 of mixed-signal components,
4 a first digital module coupled to the analog module, the first digital module
5 having a first plurality of digital components required for functional/parametric
6 verification of the plurality of mixed-signal components within the partitioned
7 analog module, wherein the first digital module provides a plurality of clocking
8 signals, a power-down control signal, a reset signal, an analog test sequence to
9 the analog module,
10 a first isolation unit including a first plurality of multiplexers, the first
11 isolation unit coupled between the analog module and the first digital module to
12 form a first virtual boundary that isolates a plurality of signals between the analog
13 module and the first digital module,
14 a second digital module having a second plurality of digital components,
15 a second isolation unit coupled between the first digital module and the
16 second digital module to form a second virtual boundary that isolates a plurality
17 of signals between the first digital module and the second digital module,
18 a partition controller coupled to the first and second digital module to
19 provide a test clock control signal, a SCAN enable control signal, a Built-in self
20 test (BIST) control signal and a mixed-signal parallel test control signal,
21 a testing clock signal generator coupled between the partition controller
22 and the first digital module to provide a clocking signal for the first digital module,
23 a top level pin multiplexing unit coupled to the analog module, the first
24 digital module, and the second digital module, to multiplex serial data internal to
25 the integrated circuit, and
26 a data multiplexer coupled to the top level pin multiplexing unit, the first
27 digital module and the second digital module,

28 wherein the structure for testing has at least three modes of operation for
29 testing the mixed-signal core, a first mode of operation that provides digital
30 interface characterization testing of the first and second digital module and
31 analog characterization/trimming testing of the analog module, wherein, in the
32 first mode of operation, the first isolation unit and the second isolation unit are
33 inactive;

34 wherein a second mode of operation that provides concurrent testing of
35 the analog module, the first digital module, and the second digital module,
36 wherein analog characterization/trimming testing is performed on the analog
37 module and digital interface characterization testing is performed on the first
38 digital module, while SCAN/BIST testing is performed on the second digital
39 module, wherein, in the second mode of operation, the second isolation unit is
40 activated to gate the plurality of signals transmitted between the first digital
41 module and the second digital module;

42 wherein a third mode of operation that provides non-concurrent testing of
43 the analog module, the first digital module, and the second digital module, the
44 third mode of operation supplies SCAN/BIST testing of the first and second
45 plurality of digital components from the first digital module and the second digital
46 module, while the analog module is powered down, and wherein, in the third
47 mode of operation, the first and second isolation units are activated to gate the
48 plurality of signals transmitted between the first digital module and the analog
49 module and to gate the plurality of signals transmitted between the first digital
50 module and the second digital module, respectively.

1 8. (currently amended) A structure for testing an integrated circuit chip having
2 an analog core, an mixed-signal core, an digital core, a microprocessor core, and
3 a memory core therein, comprising:

4 wherein the mixed-signal core comprises;

5 an analog module having a plurality of analog components and a
6 plurality of mixed-signal components,

7 a first digital module coupled to the analog module, the first digital
8 module having a first plurality of digital components required for
9 functional/parametric verification of the plurality of mixed-signal
10 components within the partitioned analog module, wherein the first digital
11 module provides a plurality of clocking signals, a power-down control
12 signal, a reset signal, an analog test sequence to the analog module,

13 a first isolation unit including a first plurality of multiplexers, the first
14 isolation unit coupled between the analog module and the first digital
15 module to form a first virtual boundary that isolates a plurality of signals
16 between the analog module and the first digital module,

17 a second digital module having a second plurality of digital
18 components,

19 a second isolation unit coupled between the first digital module and
20 the second digital module to form a second virtual boundary that isolates
21 a plurality of signals between the first digital module and the second digital
22 module,

23 a partition controller coupled to the first and second digital module
24 to provide a test clock control signal, a SCAN enable control signal, a
25 Built-in self test (BIST) control signal and a mixed-signal parallel test
26 control signal,

27 a testing clock signal generator coupled between the partition
28 controller and the first digital module to provide a clocking signal for the
29 first digital module,

a top level pin multiplexing unit coupled to the analog module, the first digital module, and the second digital module, to multiplex serial data internal to the integrated circuit, and

a data multiplexer coupled to the top level pin multiplexing unit, the first digital module and the second digital module,

wherein the structure for testing has at least three modes of operation for testing the mixed-signal core, a first mode of operation that provides digital interface characterization testing of the first and second digital module and analog characterization/trimming testing of the analog module, wherein, in the first mode of operation, the first isolation unit and the second isolation unit are inactive;

wherein a second mode of operation that provides concurrent testing of the analog module, the first digital module, and the second digital module, wherein analog characterization/trimming testing is performed on the analog module and digital interface characterization testing is performed on the first digital module, while SCAN/BIST testing is performed on the second digital module, wherein, in the second mode of operation, the second isolation unit is activated to gate the plurality of signals transmitted between the first digital module and the second digital module;

wherein a third mode of operation that provides non-concurrent testing of the analog module, the first digital module, and the second digital module, the third mode of operation supplies SCAN/BIST testing of the first and second plurality of digital components from the first digital module and the second digital module, while the analog module is powered down, and wherein, in the third mode of operation, the first and second isolation units are activated to gate the plurality of signals transmitted between the first digital module and the analog module and to gate the plurality of signals transmitted between the first digital module and the second digital module, respectively;

wherein the microprocessor core for executing microprocessor instructions multiple times and evaluating the results to ensure integrity of the

60 microprocessor core and for testing the memory core by generating a memory
61 test pattern by the memory core and evaluating the results; and

62 a host computer for providing an executable test program to the
63 microprocessor core through an interface circuit;

64 wherein the analog module and the first digital module are provided with a
65 test pattern for characterization testing generated by the microprocessor core
66 and the resultant output of the analog module and the first digital module are
67 evaluated by either the microprocessor core or the host computer;

68 wherein the first and second digital module are provided with a test
69 pattern for SCAN/BIST testing generated by the microprocessor core and the
70 resultant output of the first and second digital module are evaluated by either the
71 microprocessor core or the host computer.

1 9. (currently amended) A structure for testing a integrated circuit chip as
2 recited in claim 8, wherein the first isolation unit comprises;

3 a clock/power-down multiplexer coupled between to the first digital
4 module and the analog module, the first clock/power-down multiplexer coupled to
5 receive the clocking signal from the first digital module and a mixed-signal
6 parallel test control signal;

7 a digital-to-analog converter (DAC) data multiplexer coupled
8 between the first digital module and the analog module, the DAC data
9 multiplexer coupled to receive the mixed-signal parallel test control signal and
10 data from the first digital module; and

11 an analog-to-digital converter (ADC) data multiplexer coupled
12 between the first digital module and the analog module, the ADC data
13 multiplexer coupled to receive the mixed-signal parallel test control signal and
14 data from the analog module.

1 10. (currently amended) A structure for testing a integrated circuit chip as
2 recited in claim 8, wherein the second isolation unit comprises;

3 a serial-to-parallel data converter coupled to receive serial data from the
4 second digital module;

5 a format converter/post processing unit coupled to the serial-to-parallel
6 converter to format and process the parallel data;

7 at least one multiplexer coupled to the format converter/post processing
8 unit, the first digital module, and the second digital module to provide an isolated
9 control interface, the at least one multiplexer coupled to receive the mixed-signal
10 parallel test control signal from the partition controller.

1 11. (currently amended) A structure for testing a integrated circuit chip as
2 recited in claim 8, wherein the testing clock signal generator comprises;

3 a digital clock controller;

4 a top level clock controller coupled to the partition controller; and

5 a clock multiplexer, having a first input, a second input, a control
6 input, and an output, to provide a multiplexed clocking signal to the first digital
7 module, the first input coupled to the top level clock controller, the second input
8 coupled to the digital clock controller, the control input coupled to the partition
9 controller, the output coupled to the first digital module.

1 12. (original) A structure for testing a integrated circuit chip as recited in claim 8,
2 wherein the test program applied to the microprocessor core is an object code of
3 assembly language test program.

1 13. (original) A structure for testing a integrated circuit chip as recited in claim 8,
2 wherein the assembly language test program is provided to the microprocessor
3 core from an external host computer through an I/O interface.

1 14. (original) A structure for testing a integrated circuit chip as recited in claim 8,
2 wherein the assembly language test program is provided to the microprocessor
3 core from an external IC tester through an I/O interface.

1 15. (original) A structure for testing a integrated circuit chip as recited in claim 8,
2 wherein the integrated circuit chip is a system-on-chip (SoC) IC.